MIPS® Malta™-R Development Platform User's Manual

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Chapter 1

Introduction

This manual describes the setup, configuration, and general operation of the Malta™-R Development Platform.

1.1 Overview

The Malta™-R Development Platform provides a robust and flexible environment for the development and testing of software based on MIPS32® and MIPS64® processor cores.

The platform is comprised of two major hardware systems: the Malta-R Motherboard that holds the CPU-independent parts of the circuitry, and one or more Core Processor Boards that hold the MIPS CPU plus its System Controller and additional support hardware. This combination allows users to evaluate and develop applications for specific MIPS32® or MIPS64® processor cores using a common development environment.

The Malta-R Motherboard connects to standard PC peripherals, making it easy for users to add more functionality, such as extra networking, hard drives, and input devices.

The Core Processor Board is an FPGA (Field Programmable Gate Array) emulation of a MIPS32 or MIPS64 core. All Core boards conform to a common interface specification, though they differ in type, depending on user requirements.

Basic operation of the Malta-R Development Platform is controlled by YAMON™ (Yet Another MONitor) supplied in the Motherboard's Flash memory. YAMON [2] allows for status to be printed, settings of both the Core Board and the Motherboard to be changed, and programs to be loaded into system RAM for execution. YAMON also provides basic boot loader capabilities to allow operating systems such as Linux to be booted from properly formatted hard drives.

The Malta-R board complies with the RoHS Directive, which restricts the use of certain hazardous substances in new electronic equipment for sale in the EU market. For more information on RoHS, refer to http://www.rohs.gov.uk.

1.2 Document Conventions

In this document, descriptions of the positions of various connectors, jumpers. and indicators on the board will be made assuming that the Malta-R Motherboard is positioned as shown in Figure 1.1.

Text relating to terminal output, memory addresses, or register bit fields is shown in `Courier` font. Descriptions of user input from the host terminal uses the following abbreviations:

<ret> - Return or enter key

<tab> - Tab key

<cntrl> or <^> - Control key

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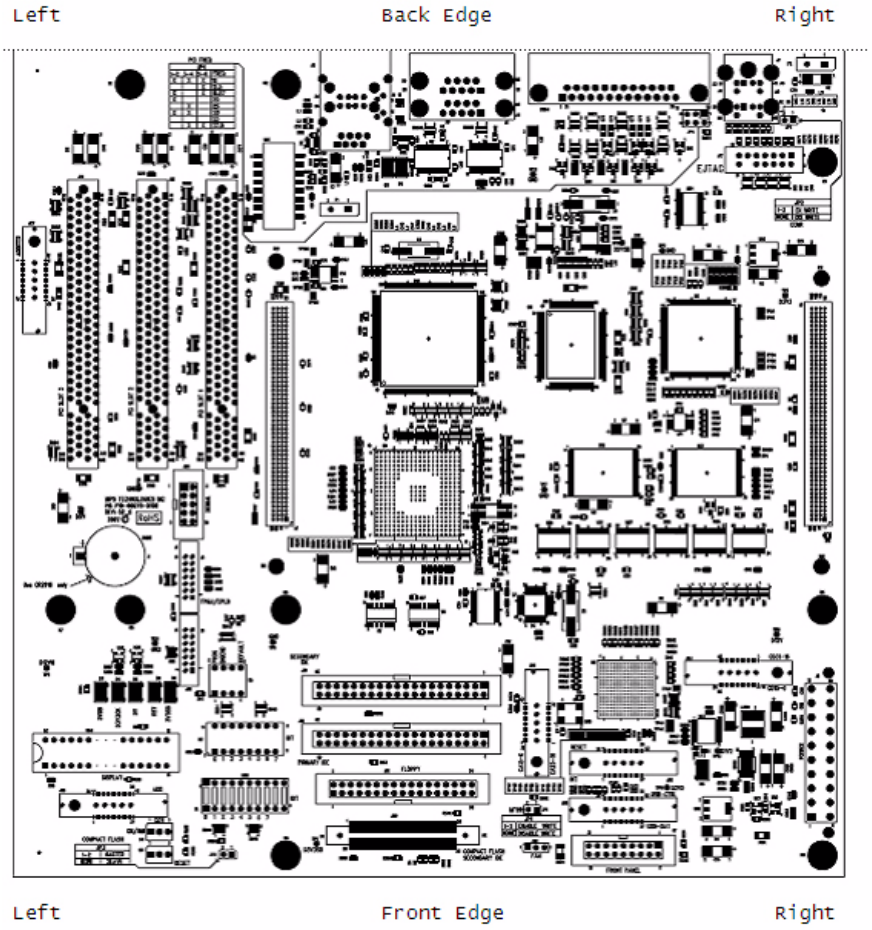
Figure 1.1 Malta™-R Board Orientation



1.3 Malta™-R Development Platform Contents

The Malta-R Development Platform contains the following components:

- Malta-R Motherboard
- Core Processor Board
- Null Modem serial cable
- Malta-R Development Platform CDROM
- Hard drive preloaded with a MIPS version of Linux, when specifically ordered
- DB25 Gender changer plug

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Chapter 2

Getting Started

This chapter describes how to get the Malta-R Development Platform up and running.

========== **WARNING** ==========

Disconnect the AC power cord from the ATX power supply before connecting anything, including the ATX 20 pin connector to the Malta-R Motherboard. The Malta-R Development Platform will power-up when it is connected to the power supply, and this may cause damage to the Motherboard or the Core Processor board if either of them is not configured or connected properly.

==========

2.1 Required Hardware

- Malta-R Motherboard with attached Core Processor Board. If the Core Processor Board is not already plugged into the Motherboard, refer to Section 2.5.1 “Core Board Insertion”.
- ATX Power Supply (300 W or greater).
- Null modem serial cable as supplied with Malta-R Platform. Specification of this cable connection can be found in Section 2.3 “Serial Cable Connection”.

2.2 Power Supply Connection

Connect the 20-pin ATX power connector to the lower right corner of the Malta-R Motherboard, again making sure that the ATX power supply is disconnected from the AC supply.

2.3 Serial Cable Connection

Connect the Null Modem serial cable to the top DB9 male serial port located on the back edge of the Malta-R Motherboard. Connect the other end of the cable to the serial port of the host PC or Workstation. The default serial communication parameters of the Malta-R Motherboard are 38400 baud, 8N1, with hardware flow control.

2.4 Power Up

Start the terminal emulation program on the host workstation and double check that the communication parameters are set to 38400 baud, 8N1, with hardware flow control.

Apply AC power to the ATX power supply and observe the power-up sequence described below. The power supply/reset status LEDs are located in the lower left-hand corner of the Motherboard just above the alphanumeric display.

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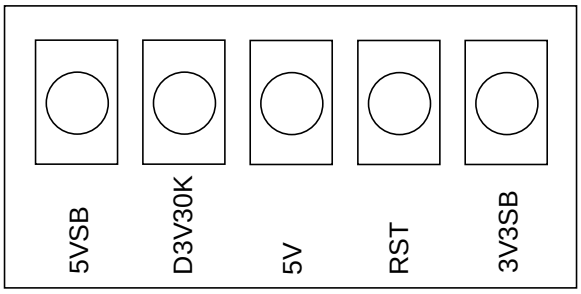
Figure 2.1 Status LED Block



Immediately after power-up, all LEDs in the status block (Figure 2.1) will turn on. After a few seconds, the RST LED will go off, indicating that a RESET cycle has been performed. The YAMON main boot screen will appear on the terminal emulation program, and then the system will wait at the YAMON command prompt. Eventually, the alphanumeric display will display:

```
YAMON 2.xx
```

where xx is the current YAMON version number (shown in the *MIPS Malta™-R Errata Sheet* [19] provided with the Malta-R Motherboard).

The following boot screen will appear in the terminal emulation program running on the host workstation:

```
YAMON ROM Monitor, Revision 02.14cm.
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For a list of available commands, type 'help'.

Compilation time =              Mar 26 2008  18:39:17 (chris)
Board type/revision =           0x02 (Malta) / 0x08
Core board type/revision =      0x0a (Core24K) / 0x00
System controller/revision =    MIPS SOC-it 101 OCP / 1.3   SDR-FW-2:1
FPGA revision =                 0x0001
MAC address =                   00.d0.a0.00.06.2d
Board S/N =                     0000000019
PCI bus frequency =             33.33 MHz
Processor Company ID/options =  0x01 (MIPS Technologies, Inc.) / 0x00
Processor ID/revision =         0x93 (MIPS 24Kc) / 0x64
Endianness =                    Little
CPU/Bus frequency =             320 MHz / 160 MHz
Flash memory size =             4 MByte
SDRAM size =                    256 MByte
First free SDRAM address =      0x800b6a20

WARNING: Environment variable 'ipaddr' is undefined!
WARNING: Environment variable 'subnetmask' is undefined!

YAMON>
```

2.5 Insertion and Removal of Core Processor Boards

The Core Processor Board and the Malta-R Motherboard are joined via 4 standoff posts and a pair of 20-pin connectors. One of the standoff posts is slightly offset to prevent incorrect insertion in the Motherboard.

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2.5.1 Core Board Insertion

Insertion of the Core Board is straightforward because the mounting holes in the Core Processor Board will only align one way. Inspect the pins of the connectors of the Core Board to ensure that no pins are broken, missing, or bent. Also inspect the mating connectors on the Motherboard to make sure that no holes are plugged with debris or broken connector pins.

After the Core Board has been aligned and pressed lightly down on top of the 200-pin connectors, press down more firmly using both hands, applying pressure directly over the two connectors. This will ensure that the boards are connected correctly and will prevent the Core Board from flexing.

2.5.2 Core Board Removal

To remove the Core Board, gently pry up the left side of the board using a smooth and preferably non-metallic tool—a tongue depressor or popsicle stick is an excellent choice. A flat-bladed screwdriver can also be used, but be careful not to damage any traces on either board. Begin at the upper left-hand corner mounting post, and when that corner is free, move to the lower left-hand corner. Once the left connector is free, the entire board can be gently wiggled from the right-hand connector.

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Chapter 3

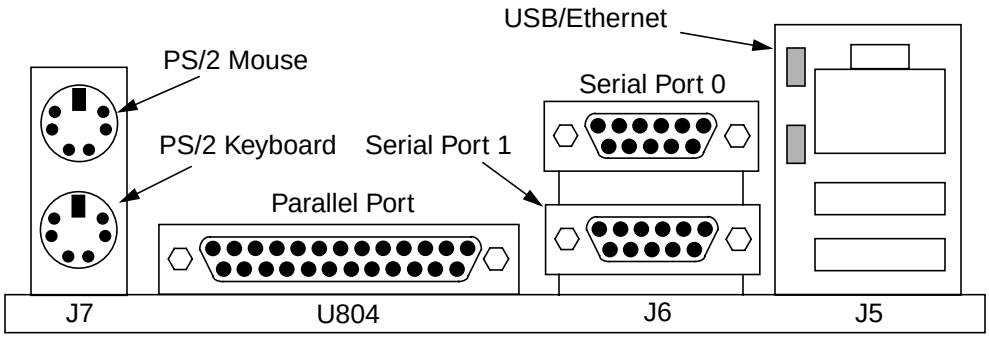
Features

The Malta™-R Motherboard provides a number of standard PC connectors to allow the user easy access to the various features of the Malta-R Development Platform. The connectors are located in two main groups. The first group is located along the back edge of the board, and the second group is located at the center of the front of the board. Several switches are also provided for control and configuration of the Platform. The system debug connectors are described in Chapter 6, “Debug Connectors” on page 37.

3.1 Back Edge Connectors

Figure 3.1 shows the back-edge connector array as viewed from the back edge. All connectors follow industry-standard pinouts and voltage levels, allowing for direct connection of the mating peripheral.

Figure 3.1 Back Edge Connectors



The connectors are described in the following subsections, from left to right.

3.1.1 J7- PS/2 Mouse and PS/2 Keyboard Connector

Connector Type: 9 DIN circular

A standard PS/2 mouse and keyboard can be connected to the Malta-R Motherboard through J7 and its pair of 9 DIN circular connectors. The keyboard connection is the port closest to the Motherboard.

This keyboard port is connected logically to the development platform via the SMS FDC37M817 SuperI/O chip (U11).

3.1.2 U804 - Parallel Port

Connector Type: DB25 Female

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U804 presents a standard 1284 printer interface that is also logically connected to the Malta-R Motherboard through the SMS FDC37M817 SuperI/O chip. This port connector is used mostly for updating YAMON.

3.1.3 J6 - RS-232 Ports

Connector Type: DB9 Male

J6 contains two standard RS-232 serial ports configured as DTE (Data Terminal Equipment), which requires that a null modem cable be used to connect either of these ports to a host PC or any other RS-232 device configured as a DTE.

3.1.4 J5 - USB / Ethernet

Connector Type: 2 USB Type B, 1 RJ -45

J5 contains both USB ports and the standard 10/100 Mbps Ethernet connection. The USB ports are driven by the USB Host controller contained in the Intel PIIX4 South Bridge device but are not natively supported by YAMON. These USB ports are available for use by operating systems booted on the Malta-R Development Platform.

There are two LED's on J5 which indicate the status of the Ethernet connection. The top green LED indicates that there is network activity, and the yellow LED below it indicates that a valid Ethernet link is present.

3.1.5 J12, J13, J14 - PCI Slots

Connector Type: 32-bit 5V PCI slot

Three PCI expansion slots are provided to add additional devices to the PCI bus. These PCI slots are described in further detail in Section 4.1.5 "J12, J13, and J14 - PCI Slots", but it is important to note here that all three of these slots are 5V only, which will accept 5V or universally-keyed PCI cards.

3.2 Front Connectors

The center front edge of the Malta-R Motherboard is dominated by the mass storage connectors which supports IDE, Floppy, and Compact Flash connections.

3.2.1 J18 - Primary IDE

Connector Type: 40 IDE .1" header

J18 presents a standard IDE interface that is logically connected to the IDE controller block of the Intel PIIX4 Southbridge chipset. This interface supports up to UDMA Mode 1 transfer rates; however ,total system throughput will depend on the type and speed of the Core Processor Board attached to the Malta-R Motherboard. This interface also supports one Master and one Slave IDE device. The connector is keyed to accept a standard 40- or 80-pin IDE cable. An 80-pin cable is recommended for use on all IDE interfaces on the Malta-R Motherboard to ensure maximum transfer rates.

The ISE interface is supported directly by YAMON in both low-level sector reads and writes, allowing for simple IDE device bootstrap operations.

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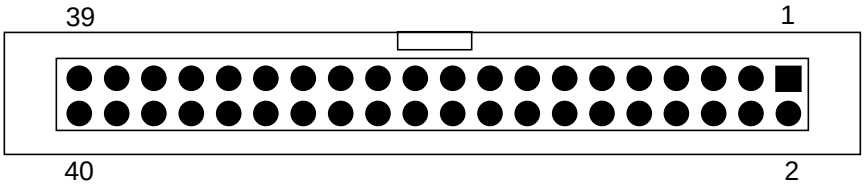
Figure 3.2 J1 - Primary IDE

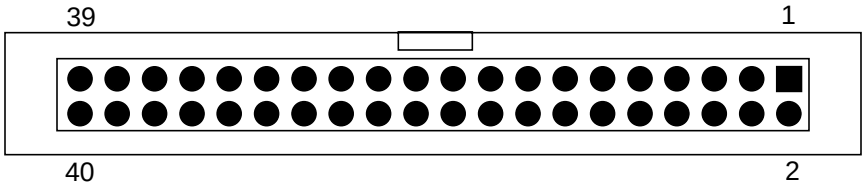


3.2.2 J19 - Secondary IDE

Connector Type: 40-pin .1” keyed header

J19 the secondary IDE channel from the PIIX4 Southbridge with all of the same features as the Primary IDE channel.

Figure 3.3 J19 - Secondary IDE



3.2.3 J21 - Floppy Drive

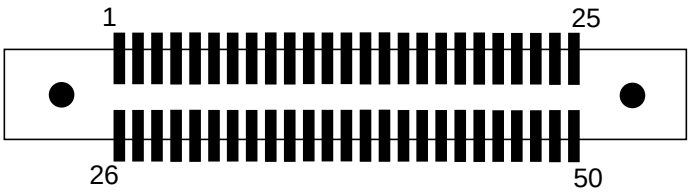
Connector Type: 34-pin .1” keyed header

J21 presents a standard PC floppy disk interface for use with either 5.25” or 3.5” floppy disk drives. This interface is provided for legacy support only through specific operating systems and is not directly supported by YAMON.

3.2.4 J20 - Compact Flash

J20 is a standard Compact Flash connector that will allow a Compact Flash device to be inserted only in the correct orientation. This connector mirrors the signals on the Secondary IDE port, so it is not recommended to have any other devices connected to the 40-pin IDE header when using the Compact Flash connector. JP3, located at the left of this connector, can be used to configure the Compact Flash device inserted into this connector as either a Master or Slave device.

Figure 3.4 J20 - Compact Flast



3.2.5 J22 - Serial Port 2

Connector Type: *Connector Type*: 2 X 5 .1” header

J22 presents a standard 2 X 5 .1” header with the following pinouts. This is the output header for UART2 which is a separate UART connected directly to the CBUS of the Malta-R board, as opposed to the UART0 and UART1 which

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are part of the SuperI/O device. The UART allows communication to the board without requiring the use of any PCI-based devices.

The signals on this connector are standard RS232-compliant.

Table 3.1 J22 - Serial Port 2

Pin	Signal
1	CD (Carrier Detect)
2	CD (Carrier Detect)
3	RX (Data Receive)
4	RTS (Request To Send)
5	TX (Data Transmit)
6	CTS (Clear To Send)
7	DTR (Data Terminal ready)
8	RI (Ring Indicator)
9	GND
10	NC

3.3 Switches

All four switches on the Malta-R Motherboard are located in the front left quadrant of the board.

3.3.1 S3 - RESET

S3 is used to perform a hard reset of the entire platform after a completed power-on cycle. This is the equivalent of a ‘warm’ reset cycle.

3.3.2 S4 - Power ON/NMI

S4 can be used as a source for an NMI interrupt or to power cycle the system similar to a standard PC. Pressing S4 momentarily will generate an NMI interrupt that will be acknowledged by the PIIX4 Southbridge, while keeping S4 depressed for approximately 5 seconds will cause the Malta-R board to power down. After a power-down cycle, the board may be repowered by pressing S4 again.

3.3.3 S2 - User Input, 8-Position Rocker DIP Switch

S2 provides a simple 8-bit switch memory mapped into the Malta-R Motherboard’s memory space (refer Figure 4.3).

3.3.4 S5 - System Configuration, 4-Position Rocker DIP Switch

S5 allows the user to configure the Malta-R board for specific operations, including Big or Little Endian selection, on-board Flash programming, and board reset. The default setting for SW5 when shipped is all OFF.

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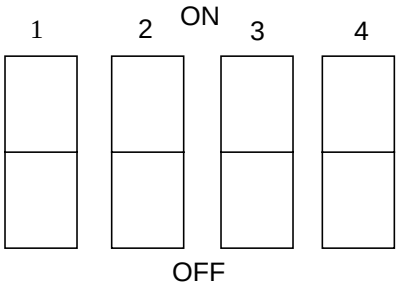
Figure 3.5 SW5 - System Configuration



3.3.4.1 SW5–1 Flash Program Enable

Default: OFF

Setting SW5-1 to ON then resetting the Malta-R Development Platform will place the board in Flash update mode. This procedure is described in detail in Chapter 4, “Malta™-R Platform System Overview” on page 21.

3.3.4.2 SW5-2 CPU Endian Selection

Default: OFF, Little Endian

Setting this switch to ON will set the board in Big Endian mode after a reboot cycle. The default mode, Little Endian, is selected by setting SW5-2 to OFF.

3.3.4.3 SW5-3 Reserved

Default: OFF

If S5-3 is enabled and an SMP/CMP processor is detected (34K/1004K), YAMON will initialise all CPUs and place them in an idle loop early on in the initialisation.

3.3.4.4 SW5-4 YAMON COM Reset

Default: OFF

SW5-4 is used to recover UART0 if communication cannot be restored to YAMON. Setting this switch to ON and then resetting the board will force UART0 to reset to the default communications parameters of 38400 baud, 8N1, with hardware flow control.

3.4 LED Displays

The majority of the Motherboard’s LED displays are located in the left front quadrant of the board, with the remaining located near the USB/Ethernet Jack and the ATX power connector.

3.4.1 D28 – 10-Position Bar LED

D28 is directly memory-mapped into the Yamon system memory space as described in Chapter 4, “Malta™-R Platform System Overview” on page 21 of this Manual.

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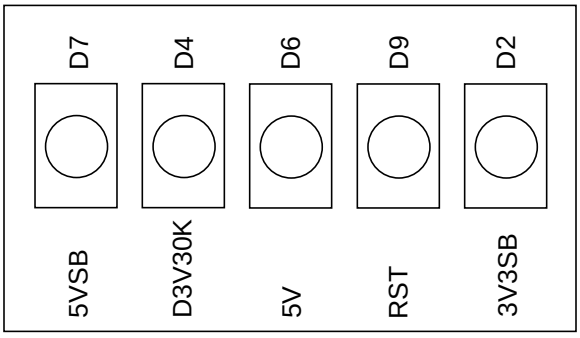
3.4.2 U42 – Dot Matrix 8 Character Display

U42 is generally used by YAMON to display board operating status. This display is also mapped in memory space as described in Chapter 4, “Malta™-R Platform System Overview” on page 21 and can be used for general display purposes by a user application.

3.4.3 D7, D4, D6, D9 and D2 – Power Status LEDs

The power and reset status LEDs are grouped together as shown in Figure 3.6.

Figure 3.6 Power Status LEDs



D7 – 5VSB

This LED indicates the status of the 5V standby voltage rail from the ATX power supply. D7 should be illuminated whenever an AC power ATX supply is connected to the Malta-R board.

D4 – D3V3OK

D4 indicates the status of the 3.3V standby voltage rail. This LED will be on whenever D7 is on and indicates proper operation of the on-board voltage regulator that creates the 3.3V voltage rail required by the Malta-R Motherboard to operate properly.

D6 – 5V

D6 indicates that the main 5V voltage rail is now present, and that the board is fully powered up and operational.

D9 – RST

D9 is on whenever a hard or soft reset signal is received by the Motherboard control logic.

D2 – 3V3SB

D2 is illuminated when both the 5V and 3.3V standby voltage rails are present and the system is able to enter a standby state as controlled by YAMON, the currently running application, or the currently running operating system. When the system enters standby mode, this LED will be OFF.

3.4.4 D5 - FPGA OK

D5 is illuminated when the System FPGA U5 has been properly configured by its serial EEPROM. This LED is ON whenever D7 and D4 are ON.

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3.4.5 D1, D3 – Ethernet Status LEDs

D1 indicates active Ethernet traffic, and D3 indicates that the Ethernet Port is operating in 100 Mb/s mode.

3.5 Jumpers

The Malta Motherboard has 5 main jumper blocks that are used to configure operation or enable firmware updates.

3.5.1 JP1- Monitor Flash Write Enable

2-position .1” pin header

ON: Monitor Flash Write is enabled

OFF: Monitor Flash Write disabled

3.5.2 JP2 - Serial EEPROM Write Enable

2-position .1” pin header

ON: Serial EEPROM Write Enable

OFF: Serial EEPROM Write Disable

This jumper is for factory programming use only.

3.5.3 JP3 - Compact Flash Master / Slave Select

2-position .1” pin header

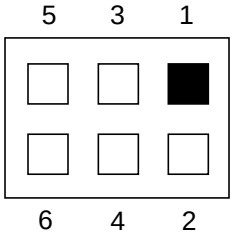
ON: Compact Flash on IDE Channel 1 assigned Master

OFF: Compact Flash on IDE channel 1 assigned Slave

3.5.4 JP4 - PCI Clock Select

2 X 3 .1” pin header

Figure 3.7 J4 - PCI Clock Select



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The jumper block JP4 is used to set the PCI clock frequency according to the values shown in Table 3.2.

Table 3.2 JP4 - PCI Clock Select

PCI Clk (MHz)	JP4 1 - 2	JP4 3 - 4	JP4 5 - 6
101.00	ON	ON	ON
12.50			ON
16.67	ON		
20.00	ON		
25.00		ON	
30.00	ON	ON	
33.00			
37.00		ON	ON

Operating the PCI bus at frequencies below 33 MHz, which is the default, will result in the Motherboard being unable to support 100 MB/s operation of the Ethernet controller. For optimal performance, it is recommended that the PCI bus frequency always be kept at 33MHz. However, some Core Boards cannot operate correctly with a PCI frequency of 33 MHz, so always consult the Core Processor User Manual for the specific maximum operating frequency.

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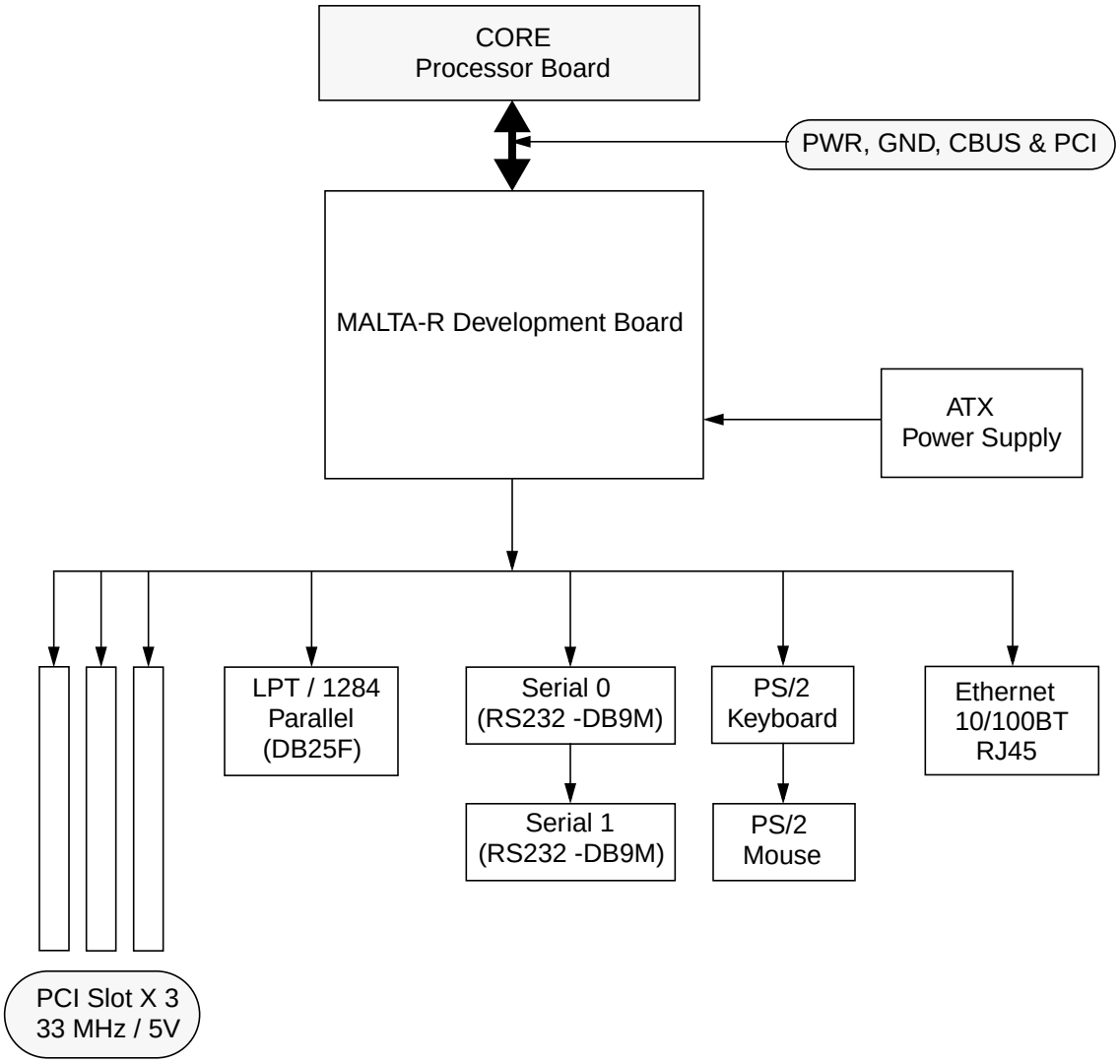
Chapter 4

Malta™-R Platform System Overview

The major components and interconnections of the Malta-R Development Platform are shown in Figure 4.1 and described in the following sections of this chapter.

Figure 4.1 Malta™-R Platform Block Diagram



4.1 Malta™-R Platform Architecture

As shown in Figure 4.2, the Malta-R Motherboard supplies the Core Processor Board with power and provides connections to the two main bus systems. The two boards are connected by the pair of 200-pin connectors, J3 and J4.

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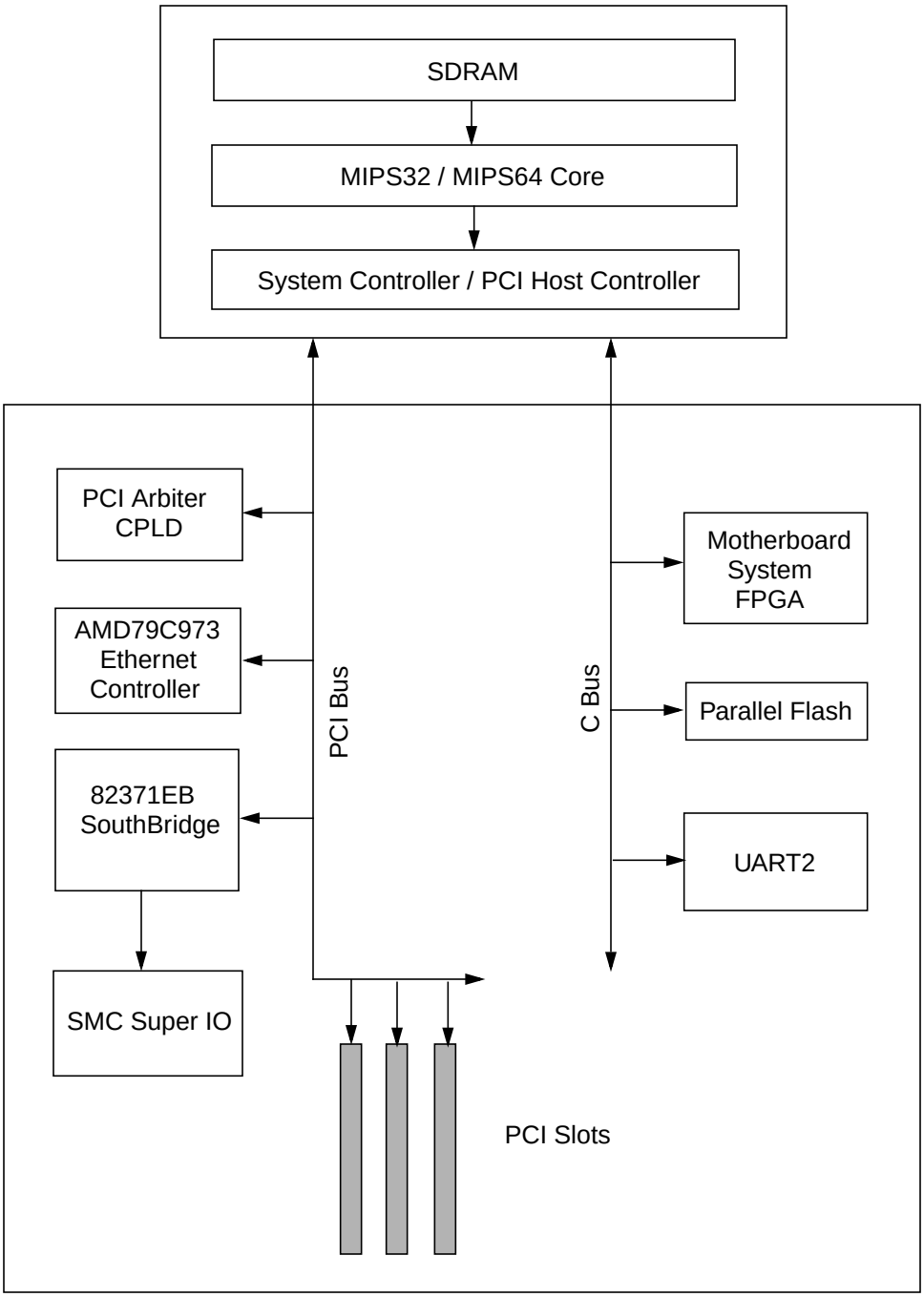
Figure 4.2 Malta™-R System Architecture



4.1.1 CBUS Interface

A core interface bus called CBUS is supplied by the Core Board and directly interfaces to the Monitor Flash device, the System FPGA device, and the third UART device

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The system FPGA (U5) defines the memory map for the entire Malta-R Development Platform, including the System Monitor Flash and the CBUS UART. Apart from exposure on some of the debug connectors, the CBUS is not made available for system expansion. Additional functionality is generally added via the PCI Bus.

4.1.2 PCI Bus Interface

The majority of the peripherals on the Malta-R Motherboard are connected to the PCI bus. A standard PCI host controller is always implemented on the Core Board connected to the Motherboard.

PCI request and grant arbitration is controlled by the CPLD (U9) which implements a round robin priority scheme.

The majority of the available I/O devices on the Malta-R Motherboard are connected to the PCI bus to provide a programming environment very similar to that of a standard PC. This allows operating system developers to take advantage of existing driver modules and stacks to quickly implement complete ports to the MIPS32 and MIPS64 Application Interface.

4.1.3 PIIX4 South Bridge

The Intel 87321EB South Bridge [8] provides the IDE, USB, Interrupt, and Timer device interfaces. This device supports two separate IDE channels with two devices per channel, along with two USB 2.0 compliant ports. Also incorporated within this device are the standard PC 8254 Timer and 8259 Interrupt Controller and real Time Clock Support.

This device is well supported by the MIPS SDE programming environment libraries and by the operating systems that have been ported to MIP32 Release 2, including Linux and Windows CE.

The 82731EB will accommodate the following devices on the PCI bus:

- ISA Bridge : Bus 0 : Device 10 : Function 0
  ```
  00:0a.0 ISA bridge: Intel Corporation 82371AB/EB/MB PIIX4 ISA (rev 02)
  ```
- IDE Controlller : Bus 0 : Device 10 : Function 1
  ```
  00:0a.1 IDE interface: Intel Corporation 82371AB/EB/MB PIIX4 IDE (rev
  01)
  ```
- USB 1.1 Host Controller : Bus 0 : Device 10 : Function 2
  ```
  00:0a.2 USB Controller: Intel Corporation 82371AB/EB/MB PIIX4 USB
  Interrupt: pin D routed to IRQ 11
  Region 4: I/O ports at 1040 [size=32]
  ```
- ACPI Controller
  ```
  00:0a.3 Bridge: Intel Corporation 82371AB/EB/MB PIIX4 ACPI
  ```

4.1.4 Ethernet Controller

Ethernet functionality is provided by the AMD AM79C973 10/100 Mbps Ethernet Controller [10] located on the PCI bus as Function 11. When the PCI bus frequency is configured to be less than 25 MHz, this Ethernet controller allows Ethernet connections to be trained at 10 Mbps; however, severe performance penalties will be noticed during normal operation.

This Ethernet controller is well supported by both Linux and the Windows CE Operating Systems and is also directly supported by the MIPS SDE environments.

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It enumerates ?? on the PCI bus as follows

- Bus 0 : Device 12 : Function 0

```
00:0b.0 Ethernet controller: Advanced Micro Devices [AMD] 79c970
[PCnet32 LANCE]
Interrupt: pin A routed to IRQ 10
Region 0: I/O ports at 1060 [size=32]
Region 1: Memory at 10100000 (32-bit, non-prefetchable) [size=32
```

4.1.5 J12, J13, and J14 - PCI Slots

The Malta-R Motherboard provides three 32-bit 5V-only PCI slots operating at a nominal frequency of 33 MHz. PCI expansion cards inserted into these slots will be properly enumerated by the PCI host controller on the Core Processor Board.

As per standard practice, the interrupt mapping between slots is rotated between the 4 PCI interrupt signals INTA#, INTB#, INTC#, and INTD#

The specific interrupt mapping for each slot is shown in Table 4.1.

Table 4.1 Interrupt Mapping

System INT	Slot 1 : J12	Slot 2 : J13	Slot 3 : J14
INTA#	INTA#	INTB#	INTC
INTB#	INTB#	INTC#	INTD#
INTC#	INTC#	INTD#	INTA#
INTD#	INTD#	INTA#	INTB#

4.1.6 Super I/O

The remaining I/O channels are supplied by the SMsC FDC37M817 Super I/O Controller [11]. This device presents two standard 16C550 UARTs and an IEEE 1284 compliant LPT port mapped to standard PC addresses.

Standard PC Mouse and Keyboard support are also provided via the dual PS/2 connectors.

4.2 Malta™-R Memory Map

The memory map for a Malta-R Development Platform is shown in Figure 4.3. Unshaded areas in the memory map are either not logically mapped to any specific device or they are reserved for internal system use.

The maximum amount of RAM usable in Malta/Core Processor board system is 256 MB.

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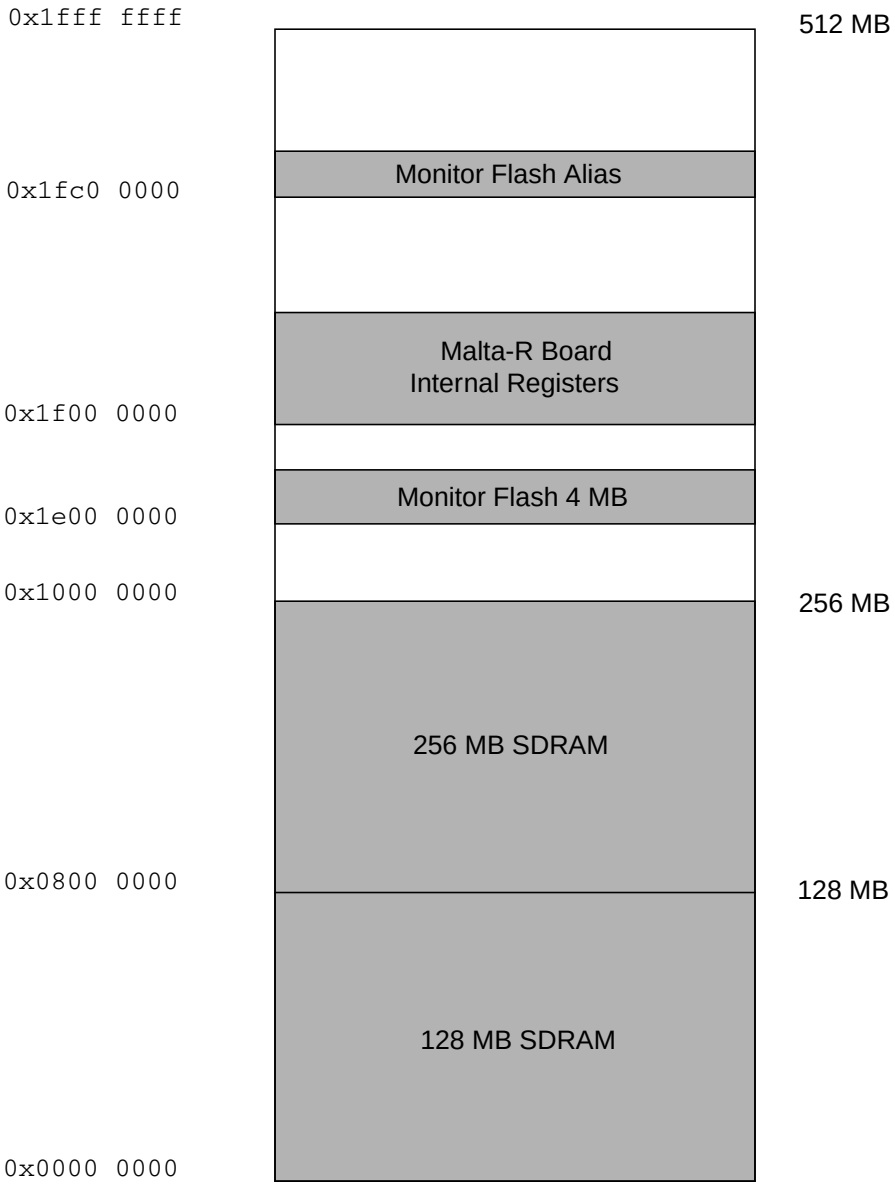
Figure 4.3 Malta™-R System Memory Map



4.2.1 SDRAM Memory Space [0x0000.0000 .. 0x0FFF.FFFF]

The SDRAM memory on the Core Processor Board is mapped to the Malta-R system memory space starting at the beginning of the kseg0/1 memory space. Depending on the amount of SDRAM memory on the Core Board,??128MB or 256 MB the entire SDRAM space is mapped linearly to 0x07FF.FFFF or 0x0FFF.FFFF respectively.

Applications built by the MIPS SDE use this memory space for both execution and data space.

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4.2.2 Monitor Flash [0x1E00.0000 .. 0x1E3F.FFFF]

The System Monitor Flash is memory mapped into Malta Memory space starting at 0x1E00 0000. This is a 32 bit wide NOR Flash device which contains the YAMON system monitor application.

4.2.3 Malta-R Internal Registers

All internal device registers are implemented within the FPGA device and are 32 bits wide and aligned on 64-bit word boundaries. The registers are summarized in Table 4.2 and described in the following subsections.

Table 4.2 Malta-R Register Summary

Register	Address	Access	Reset Value
Revision	0x1FC0.0010	RO	n/a
NMISTATUS	0x1F00.0024		
NMIACK	0x1F00.0104	WO	
SWITCH	0x1F00.0200	RO	
STATUS	0x1F00.0208		
JMPRS	0x1F00.0210		
LEDBAR	0x1F00.0408	R/W	0
ASCIIWORD	0x1F00.0410	WO	n/a
ASCIIPOS0-7	0x1F00.0410 to 0x1F00.0450	WO	n/a
SOFTRES	0x1F00.0500		0
BRKRES	0x1F00.0508	R/W	0x0A

4.2.3.1 Revision Register

The Revision register contains information about the revision of the Malta and Core Boards.

Table 4.3 Revision Register

Bits	Field Name	Function	Initial Value
31:24	Reserved	Reserved	n/a
23:16	FPGRV	FPGA Bitfile Revision	n/a
15:10	CORID	Core Board ID	n/a
9:8	PROID	Product ID	n/a
3:0	PRORV	Product Revision	n/a

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4.2.3.2 NMISTATUS Register

When the ON/NMI push button is activated, the signal is debounced and latched in the NMI interrupt controller. The South Bridge NMI is routed through the NMI controller as it is. These signals then generate an active state on the NMIN pin of the MIPS Core Board. The NMISTATUS register can be read to determine the cause of the NMI.

Table 4.4 NMISTATUS Register

Bits	Field Name	Function	Initial Value
31:2	Reserved	Reserved	n/a
1	FPGRV	NMI Pending from SouthBridge	n/a
0	CORID	NMI Pending from SW4	n/a

4.2.3.3 NMI Acknowledge Register

The ON/NMI interrupt is by nature transient. Therefore it is debounced and latched and thereafter treated as an ordinary level-based interrupt in the NMI interrupt controller. The NMI interrupt can be cleared by writing a “1” to the NMIACK register. Note that South Bridge NMI is acknowledged in the South Bridge

Note that South Bridge NMI is acknowledged in the South Bridge.

Table 4.5 NMI Acknowledge Register

Bits	Field Name	Function	Initial Value
31:1	Reserved	Reserved	n/a
0	NMIACK	NMI acknowledge	n/a

4.2.3.4 SWITCH Register

Table 4.6 SWITCH Register

Bits	Field Name	Function	Initial Value
31:8	Reserved	Reserved	n/a
7:0	NMIACK	Byte Image of 8 pos DIP switch, SW2	n/a

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4.2.3.5 STATUS Register

Table 4.7 STATUS Register

Bits	Field Name	Function	Initial Value
31:5	Reserved	Reserved	n/a
4	MFWR	Monitor Flash lock bit	n/a
3	SW5-4	Status of DIP Switch 5 bit 4	n/a
2	SW5-3	Status of DIP Switch 5 bit 3	n/a
1	SW5-2	Status of DIP Switch 5 bit 2	n/a
0	Reserved	Reserved	n/a

4.2.3.6 JMPRS Register

Table 4.8 JMPRS Register

Bits	Field Name	Function	Initial Value
31:5	Reserved	Reserved	n/a
4:2	PCICLK	Reflects the PCI Clock frequency settings as configured by the Jumper Block JP4. See Section 3.5 ?? for a complete description of this bitfield and the associated jumpers settings used for setting the PCI Clock frequency	n/a
1	EELOCK	I^2C EEPROM Lock Protect	n/a
0	Reserved	Reserved	n/a

4.2.3.7 LEDBAR Register

Table 4.9 LEDBAR Register

Bits	Field Name	Function	Initial Value
31:8	Reserved	Reserved	0
7:0		LEDBAR Bit 7 -> LEDBAR Bit 0 D28 1 - LED ON	0

4.2.3.8 ASCIIWORD Register

Table 4.10 ASCIIWORD Register

Bits	Field Name	Function	Initial Value
31:0	HEX	Hex number to be displayed. Any 32-bit value written to this register location will be displayed in its ASCII hex equivalent on the LED Display D28.	n/a

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4.2.3.9 ASCIIPOS0 - ASCIIPOS7 Registers

Table 4.11 ASCIIPOS0-7 Registers

Bits	Field Name	Function	Initial Value
31:8	Reserved	Reserved	n/a
7:0	ASCII Character Data	Each character of the ACSII display can be addressed individually via these registers. POS0 is the leftmost digit in display D28.	n/a

4.2.3.10 SOFTRES Register

Table 4.12 SOFTRES Register

Bits	Field Name	Function	Initial Value
31:8	Reserved	Reserved	n/a
7:0	RESET	Writing the value of 0x42 to the RESET field will initiate a board reset cycle.	0

4.2.3.11 BRKRES Registe

Table 4.13 BRKRES Register

Bits	Field Name	Function	Initial Value
31:8	Reserved	Reserved	0
7:0	WIDTH	This field specifies the length of a ‘BREAK’ condition on UART0 required to trigger a board reset cycle. This is used to reset the board remotely when only a serial connection is available.	0x0A (i.e., 10ms)

4.2.4 CBUS UART

A separate UART is available that is memory-mapped onto the CBUS as opposed to the PCI bus. This UART is available for use in systems that do not need or wish to use the PCI functionality of the Malta-R Board.

This UART is implemented using a standard 16C550 class device with a reference clock frequency of 3.6864 MHz. The base address of this UART located at 0x1F00.0900

The complete register set is mapped as follows. As per the standard programming interface for a 16C550 class UART, all registers are 8 bits wide, but in this case are located on 64-bit boundaries to permit faster access times.

Table 4.14 UART Registers

Register	Offset	Type	Function
RXTX	0x0000	R/W	Character Receive / Transmit register
INTEN	0x0008	R/W	Interrupt Enable register

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Table 4.14 UART Registers (Continued)

Register	Offset	Type	Function
IIFIFO	0x0010	R/W	Interrupt ID / FIFO Control
LCTRL	0x0018	R/W	Line Control register
MCTRL	0x0020	R/W	Modem Control register
LSTAT	0x0028	R/W	Line Status register
MSTAT	0x0030	R/W	Modem Status register
SCRATCH	0x0038	R/W	Scratch Working register

4.3 Interrupt Configuration

Not including the PCI interrupt structure as defined in the previous section there are two remaining interrupt topologies present on the Malta-R System. The core processor interrupt present between the Core Processor Module and the Motherboard as follows.

Table 4.15 Interrupt Configuration

CPU INT Id	Source
NMI	PIIX4 82371AB NMI / SW4
0	PIIX4 82371AB INTR
1	PIIX4 82371AB SMI
2	CBUS UART
3	COREHI
4	CORELO
5	Reserved

This above interrupt mapping is defined by the hardware design of the Core Processor Modules and the Motherboard. Logically however the standard PC IRQ environment is configured by the system as shown in Table 4.16per the following table.

Table 4.16 PC IRQ Environment

IRQ #	Source
0	System Timer, PIIX4 82371AB SouthBridge
1	Keyboard, FDC37M817 Super I/O
2	Reserved for Cascade
3	UART1, FDC37M817 Super I/O
4	UART0, FDC37M817 Super I/O
5	Not Used
6	Floppy Disk, FDC37M817 Super I/O
7	Parallel Port, FDC37M817 Super I/O
8	Real Time Clock, PIIX4 82371AB SouthBridge

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Table 4.16 PC IRQ Environment (Continued)

IRQ #	Source
9	I 2 Bus, PIIX4 82371AB SouthBridge
10	PCI INTA#, INTB#, Ethernet Controller
11	PCI INTC#, INTD#, USB Controller PIIX4 82371AB SouthBridge
12	Mouse
13	Reserved
14	Primary IDE, PIIX4 82371AB SouthBridge
15	Secondary IDE, PIIX4 82371AB SouthBridge

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Chapter 5

Using the Malta-R™ Development Platform

The Malta-R Development Platform provides a familiar programming environment for developing and testing applications for MIPS32® and MIPS64® processor cores. The following sections assume that the user is familiar with the MIPS SDE (Software Development Environment) and has successfully compiled applications targeted for the specific MIPS core that is configured in the Core Processor Module.

The Yamon User's Manual [2] provides a comprehensive explanation of all YAMON operations. Some of the more key operations and commands are described in this section. In addition, the user may have been supplied with a hard drive that contains a MIPS-specific version of Linux.

5.1 Basic Configuration

Two important basic operations of the Malta-R board are configuring the serial and Ethernet ports. Because the default speed of the serial port is only 38400 baud, the speed should be increased to the maximum of 115200 to allow for faster program transfers.

The current setting of the tty0, the main serial port, can be displayed using the `setenv` command:

```
YAMON> setenv

baseboardserial (RO)   0000000019
boot            (USER) disk read hda 3f 100 800d0000; go 800d0000
bootfile        (R/W)
bootprot        (R/W)  tftp
bootserport     (R/W)  tty0
bootserver      (R/W)  0.0.0.0
cpuconfig       (R/W)
ethaddr         (RO)   00.d0.a0.00.06.2d
fpu             (R/W)
gateway         (R/W)  192.168.64.1
ipaddr          (R/W)  192.168.70.54
memsize         (RO)   0x10000000
modetty0        (R/W)  38400,n,8,1,hw
modetty1        (R/W)  38400,n,8,1,hw
prompt          (R/W)  YAMON
softendian      (R/W)  Hardware
start           (R/W)
startdelay      (R/W)
subnetmask      (R/W)  255.255.248.0
yamonrev        (RO)   02.14cm
```

We can see that the `modetty0` variable is set to `38400`, `n`, `8`, `1`, `hw`. To change the baud rate, update the environment variable using the `setenv` command:

```
YAMON> setenv modetty0 115200,n,8,1,hw
```


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After this command returns to the command prompt, the board must be reset to allow the changes to take effect. Now is a good time to change the communication speed settings on the host terminal emulation application so that the speeds of both systems match.

```
YAMON> setenv

baseboardserial (RO)   0000000019
bootfile        (R/W)
bootprot        (R/W)  tftp
bootserport     (R/W)  tty0
bootserver      (R/W)  0.0.0.0
cpuconfig       (R/W)
ethaddr         (RO)   00.d0.a0.00.06.2d
fpu             (R/W)
gateway         (R/W)  192.168.64.1
ipaddr          (R/W)  192.168.70.54
memsize         (RO)   0x10000000
modetty0        (R/W)  115200,n,8,1,hw
modetty1        (R/W)  38400,n,8,1,hw
prompt          (R/W)  YAMON
softendian      (R/W)  Hardware
start           (R/W)
startdelay      (R/W)
subnetmask      (R/W)  255.255.248.0
yamonrev        (RO)   02.14cm

YAMON>
```

The `setenv` command is also used to configure the Ethernet settings. For example, to set the IP Address to the value shown in the above example:

```
YAMON> setenv ipaddr 192.168.70.54
```

5.2 Downloading and Running Applications

The most basic function of the Malta-R Development Platform is the ability to download and execute applications that were compiled by the MIPS SDE.

The following sequence can be used to download the `hellosa.s3` application into the Malta-R board. Begin the download sequence by setting up the Malta-R system to receive a file:

```
YAMON> load asc:
About to load asc://tty0
Press Ctrl-C to break
Start dump from terminal program
```

Use the ASCII file transfer function of the host terminal program to begin the download. For Windows HyperTerminal, use “Transfer -> Send text File”. For Minicom under Linux, use CNTRL-A S. The file will begin downloading automatically. The ACSII display on the Malta-R board will increment quickly, displaying the memory addresses being written as the file is downloaded.

```
Start = 0x80100000, range = (0x80100000,0x801016ef), format = SREC
YAMON>
```

The application can now be executed using the `go` command:

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```
YAMON> go
Hello World!
User application returned with code = 0x00000000
YAMON>
```

5.3 Booting an Operating System

Booting an operating system requires that a disk boot loader application be loaded into memory and then executed. This is a two-step process that can be combined into a single environment variable macro.

The following command will define a YAMON environment variable called `boot` which will perform a direct disk read into a specific memory location and then execute the boot loader application that was loaded.

```
YAMON> setenv boot "disk read hda 3f 100 800d0000; go 800d0000"
```

The new environment command can now be executed:

```
YAMON> $boot
```

Below is the screen output from executing the boot command on a hard drive loaded with a TimeSys Linux release.

```
Loading /boot/mb.conf . ok
Choose a kernel image to boot:
  (0) smvp-2.6.19-glibc         root=/dev/hda3
  (1) aprp-2.6.19-glibc         root=/dev/hda3
  (2) smtc-2.6.19-glibc         root=/dev/hda3
  (3) exp-aprp-2.6.20-glibc     root=/dev/hda3
  (4) exp-smtc-2.6.20-glibc     root=/dev/hda3
  (5) exp-smvp-2.6.20-glibc     root=/dev/hda3
  (6) smvp-2.6.19-uclibc        root=/dev/hda9
  (7) aprp-2.6.19-uclibc        root=/dev/hda9
  (8) smtc-2.6.19-uclibc        root=/dev/hda9
  (9) exp-aprp-2.6.20-uclibc    root=/dev/hda9
 (10) exp-smtc-2.6.20-uclibc    root=/dev/hda9
 (11) exp-smvp-2.6.20-uclibc    root=/dev/hda9
 (12) 2.6.19-glibc-r1           root=/dev/hda7
or e(x)it back to YAMON
: 0
Loading /boot/vmlinux-kernel-smvp-2.6.19-malta.13
.. ok

LINUX started...
Config serial console: console=ttyS0,115200n8r
Linux version 2.6.19.1smvp (root@bslave2-4.timesys.com) (mipsisa3
```

5.4 Updating the Monitor Flash (YAMON)

In order to support more complex Core Processor Module configurations or to address general maintenance of YAMON, the Malta-R board provides this facility using the host workstation parallel port. These operations are most easily performed on a Linux-based workstation with a standard DB25 parallel port configured as lp0.

The new YAMON image will be submitted as a `.fl` file, which is an ASCII file containing specific character sequences and commands along with an ASCII representation of the new YAMON Monitor.

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To perform a monitor Flash upgrade:

- Using a standard DB25 parallel printer cable and the gender changer supplied with the Malta-R kit, connect the Malta-R Motherboard to the host workstation. The gender changer is required to create a straight-through DB25 male to DB25 male cable. Do not use a DB25 modem cable for this operation, because the signal connections between the two DB25 connectors are not guaranteed to be correct.
- Switch off power to the Malta-R board, and then set SW-1 to the ON position.
- Power on the Malta-R Board and confirm that "`Flash DL`" appears in the LED ASCII display. This indicates that the proper programming mode has now been initialized.
- Use the following command to transfer the `yamon-xxxx.fl` to the printer port:

```
sde_dev/~ %cat yamon-2.14cmp.fl > /dev/lp0
```

- The ASCII LED display will show brief updates of incrementing memory addresses until "FINISHED" is displayed.
- Power off the Malta-R System, set SW-1 back to the default OFF position, and boot the new YAMON Monitor.

In some cases, loading a new YAMON image may cause the default serial port settings to return, so if there is garbled output on the terminal emulator application, these communication settings will need to be changed to view the correct YAMON serial output.

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Chapter 6

Debug Connectors

The Malta-R Motherboard provides a large number of debug connectors that allow direct access to both logical debug ports and to logic signals present on the Malta-R Motherboard. Debug visibility can be divided into three major groups: JTAG, PCI, and CBUS.

6.1 J17 - EJTAG Debug Connector

JTAG debugging is provided through a standard 14-pin .1” pin header located in the back right quadrant of the Motherboard near the PS/2 mouse and keyboard connector. MIPS cores provide a specific variant of the JTAG interface known as EJTAG; however, the physical signals and pin assignments are backwards-compatible with standard JTAG hardware systems.

The standard pinout for J17 is shown in Figure 6.1 and described in Table 6.1.

Figure 6.1 J17 – EJTAG Connector

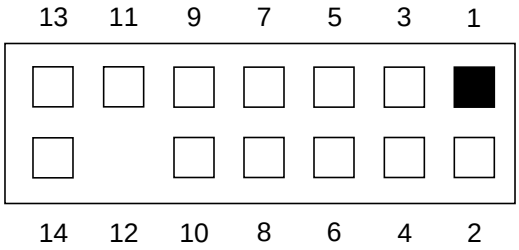

Table 6.1 J17 - EJTAG Connector

Pin	Signal	Description
1	TRSTn	Target Reset
2	GND	Signal Ground
3	TDI	Target Debug Input
4	GND	GND
5	TDO	Target Debug Output
6	GND	Signal Ground
7	TMS	Target Mode Select
8	GND	Signal Ground
9	TCK	Target Clock
10	GND	Signal Ground
11	RSTn	JTAG Reset

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Table 6.1 J17 - EJTAG Connector (Continued)

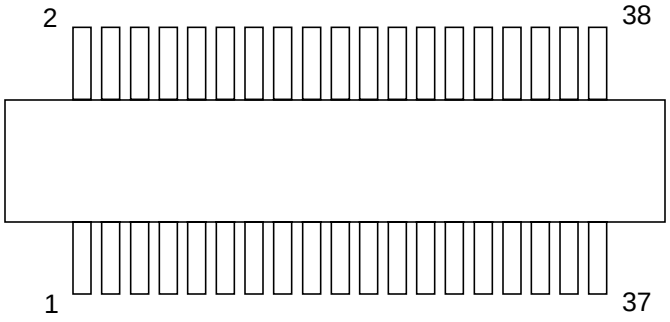
Pin	Signal	Description
12	N/C	Not Connected
13	INT	JTAG Interrupt
14	GND	Signal Ground

6.2 Logic Analyzer Connections

A significant number of debug signals are presented on the 5 Mictor connectors on the Malta-R Motherboard. All Mictor connectors are configured as per the HP Logic Analyzer standard to simplify configuration of channel identification. When using Logic Analyser systems from other manufacturers, consult the following tables carefully to avoid damage to either the test equipment or the Malta-R Motherboard.

Mictor connectors follow the standard pin number convention as shown in Figure 6.2. The connectors are keyed such that the mating half from the logic analyzer can only be inserted one way; however, always confirm where Pin 1 is on the specific Mictor used on the Malta-R board.

Figure 6.2 Mictor Connector



Pinouts of the Mictor connectors are presented in 4 columns, representing the odd and even rows of pins respectively.

6.2.1 J27 - PCI Arbiter, 38-Pin Mictor

J27 is located near the last PICI connector to allow easy access to all the PCI control signals and standard PCI bus signals (by way of a PCI Logic Analyzer breakout card, which is not supplied).

Table 6.2 J23 - PCI Arbiter

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	40 MHz Clock	6	PCI_CLK_ARBITER
7	NC	8	PCI_REQ#_CORE
9	NC	10	PCI_REQ#_SOUTHBRIDGE
11	NC	12	PCI_REQ#_ETHERNET
13	NC	14	NC

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Table 6.2 J23 - PCI Arbiter (Continued)

Pin	Signal	Pin	Signal
15	NC	16	PCI_REQ#_CON1
17	NC	18	PCI_REQ#_CON2
19	PCI_INTA#	20	PCI_REQ#_CON3
21	PCI_INTB#	22	NC
23	PCI_INTC#	24	PCI_GNT#_CORE
25	PCI_INTD#	26	PCI_GNT#_SOUTHBRIDGE
27	PCI_FRAME#	28	PCI_GNT#_ETHERNET
29	PCI_IRDY#	30	NC
31	PCI_TRDY#	32	PCI_GNT#_CON1
33	PCI_DEVSEL#	34	PCI_GNT#_CON2
35	PCI_STOP#	36	PCI_GNT#_CON3
37	PCI_LOCK#	38	NC

6.2.2 J23 - CBUS Data

Table 6.3 J23 - CBUS Data

Pin	Signal	Pin	Signal
1	NC	2	CBUS_D18
3	GND	4	CBUS_D17
5	40 MHz Clock	6	CBUS_D16
7	CBUS_D31	8	CBUS_D15
9	CBUS_D30	10	CBUS_D14
11	CBUS_D29	12	CBUS_D13
13	CBUS_D28	14	CBUS_D12
15	CBUS_D27	16	CBUS_D11
17	CBUS_D26	18	CBUS_D10
19	CBUS_D25	20	CBUS_D09
21	CBUS_D24	22	CBUS_D08
23	CBUS_D23	24	CBUS_D07
25	CBUS_D22	26	CBUS_D06
27	CBUS_D21	28	CBUS_D05
29	CBUS_D20	30	CBUS_D04
31	CBUS_D19	32	CBUS_D03
33	CBUS_D18	34	CBUS_D02
35	CBUS_D17	36	CBUS_D01
37	CBUS_D16	38	CBUS_D00

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6.2.3 J24 - CBUS Address and Control

Table 6.4 J24 - CBUS Address and Control

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	CLK_1KHZ	6	CLK_32KHZ
7	FPGA_RSTn	8	CBUS_A15
9	RSTn	10	CBUS_A14
11	BIGEND	12	CBUS_A13
13	CBUS_WRn	14	CBUS_A12
15	CBUS_RDn	16	CBUS_A11
17	CBUS_CSn	18	CBUS_A10
19	CBUS_A25	20	CBUS_A09
21	CBUS_A24	22	CBUS_A08
23	CBUS_A23	24	CBUS_A07
25	CBUS_A22	26	CBUS_A06
27	CBUS_A21	28	CBUS_A05
29	CBUS_A20	30	CBUS_A04
31	CBUS_A19	32	CBUS_A03
33	CBUS_A18	34	CBUS_A02
35	CBUS_A17	36	GND
37	CBUS_A16	38	GND

6.2.4 J25 - CBUS Control, ASCII Display Data, and Address

Table 6.5 J25 - CBUS Control, ASCII Display Data and Address

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	CLK_40MHZ	6	NC
7	FRSTn	8	IIC_SCL
9	PAR_ENAB	10	IIC_SDA
11	FPGA_RSTn	12	NC
13	MFSTS	14	ADA4
15	UCSn	16	ADA3
17	REVCSn	18	ADA2
19	CGPIOCSn	20	ADA1
21	CGPIOWR	22	ADA0

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Table 6.5 J25 - CBUS Control, ASCII Display Data and Address (Continued)

Pin	Signal	Pin	Signal
23	MFCSn	24	ADD7
25	ASWCSn	26	ADD6
27	ADCSn	28	ADD5
29	ABRLEDCS	30	ADD4
31	NC	32	ADD3
33	NC	34	ADD2
35	NC	36	ADD1
37	NC	38	ADD0

6.2.5 J28 - USB, Parallel Port, and FPGA

Table 6.6 J28 - USB, Parallel Port, and FPGA

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	NC	6	PAR_BUSY
7	USB_RDn	8	USB_A15 (4K7 to GND)
9	USB_WRn	10	USB_A14 (4K7 to GND)
11	PAR_STROBEn	12	USB_A13 (4K7 to GND)
13	PAR_BUSY	14	USB_A12 (4K7 to GND)
15	PAR_ENAB	16	USB_A11 (4K7 to GND)
17	USB_ENAB	18	USB_A10 (4K7 to GND)
19	NC	20	USB_A9 (4K7 to GND)
21	NC	22	USB_A8 (4K7 to GND)
23	PARA_F_DATA7	24	FPGA_EPLD7
25	PARA_F_DATA6	26	FPGA_EPLD6
27	PARA_F_DATA5	28	FPGA_EPLD5
29	PARA_F_DATA4	30	FPGA_EPLD4
31	PARA_F_DATA3	32	FPGA_EPLD3
33	PARA_F_DATA2	34	FPGA_EPLD2
35	PARA_F_DATA1	36	FPGA_EPLD1
37	PARA_F_DATA0	38	FPGA_EPLD0

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6.2.6 J26 - RESET and Status

Table 6.7 RESET and Status

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	NC	6	PAR_BUSY
7	USB_RDn	8	USB_A15 (4K7 to GND)
9	USB_WRn	10	USB_A14 (4K7 to GND)
11	PAR_STROBEn	12	USB_A13 (4K7 to GND)
13	PAR_BUSY	14	USB_A12 (4K7 to GND)
15	PAR_ENAB	16	USB_A11 (4K7 to GND)
17	USB_ENAB	18	USB_A10 (4K7 to GND)
19	NC	20	USB_A9 (4K7 to GND)
21	NC	22	USB_A8
23	PARA_F_DATA7	24	FPGA_EPLD7
25	PARA_F_DATA6	26	FPGA_EPLD6
27	PARA_F_DATA5	28	FPGA_EPLD5
29	PARA_F_DATA4	30	FPGA_EPLD4
31	PARA_F_DATA3	32	FPGA_EPLD3
33	PARA_F_DATA2	34	FPGA_EPLD2
35	PARA_F_DATA1	36	FPGA_EPLD1
37	PARA_F_DATA0	38	FPGA_EPLD0

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Appendix A

References

This appendix lists other documents available from MIPS Technologies, Inc. that are referenced elsewhere in this document. These documents may be included in the `$MIPS_HOME/$MIPS_CORE/doc` area of a typical *CoreName* soft or hard core release, or in some cases may be available on the MIPS web site, http://www.mips.com.

1. PCI Local Bus Specification
   Revision 2.2. December 18, 1998

2. MIPS® YAMON™ User's Manual
   MIPS Document: MD00008

3. MIPS® YAMON™ Reference Manual
   MIPS Document: MD00009

4. MIPS® EJTAG Specification
   MIPS Document: MD00047

5. MIPS® CoreFPGA™ 4 User's Manual
   MIPS Document: MD00569

6. MIPS® CoreFPGA™ 5 User's Manual
   MIPS Document: MD00632

7. 24KEc™ Reference Design for CoreFPGA™ 4B Board
   MIPS Document: MD00631

8. Intel 82371EB (PIIX4E) South Bridge Chipset Datasheets
   http://www.intel.com

9. Crystal CS4281 Audio Controller Datasheet
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10. AMD 79C973 Ethernet Controller Datasheet
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11. SMSC FDC37M817 Super I/O Controller Datasheet

12. Texas Instruments TI16C550C UART Datasheet
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13. Intel ATX Power Supply Design Guide. Version 0.9
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14. ATX Specification 2.03
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15. Design Guide for Intel ATX Motherboard I/O Implementations. Version 1.1
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18. MIPS® Malta™-R Development Platform Schematics
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19. MIPS® Malta™-R Development Platform Errata Sheet
MIPS Document: MD000628

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Appendix B

Revision History

Change bars (vertical lines) in the margins of this document indicate significant changes in the document since its last release. Change bars are removed for changes that are more than one revision old.

Revision	Date	Description
01.00	May 30, 2008	Initial release.
01.01	August 28, 2009	Update with new functionality of S5-3 switch.

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